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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/679,115	10/04/2000	Theodore Calderone	AGLE0003	7284

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GLENN PATENT GROUP  
3475 EDISON WAY, SUITE L  
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EXAMINER
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O BRIEN, BARRY J

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/679,115

Applicant(s)

CALDERONE ET AL.

Examiner

Barry J. O'Brien

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 10/04/00 to 4/08/02.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-92 is/are pending in the application.
- 4a) Of the above claim(s) 31-92 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 10/04/00 - 4/08/02.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

**DETAILED ACTION**

1. Claims 1-30 have been examined.

***Papers Submitted***

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: IDS as received on 10/04/00, IDS as received on 1/03/01, IDS as received on 2/05/01, Drawings as received on 2/09/01, IDS as received on 5/22/01, IDS as received on 7/20/01, IDS as received on 12/18/01 and IDS as received on 4/08/02.

***Election/Restrictions***

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:
  - I. Claims 1-30, drawn to the structure of a communications mesh, classified in class 712, subclass 13.
  - II. Claims 31-42, drawn to a method of communicating, classified in class 370, subclass 464.
  - III. Claims 43-92, drawn to routing of communications, classified in class 709, subclass 238.
4. The inventions are distinct, each from the other because of the following reasons:  
Inventions I, II and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention Group II has separate utility such as a method of communicating between nodes and node pencils involving traversing physical transport layers,

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with the method being able to be used in any communication grid structure, as long as said grid has multiple nodes and communication pencils, and does not require the specific structure of Group I. Group III has separate utility such as inter-nodal communication being controlled by communications interfaces in order to send local communications, and the method of communications can be applied to any communications grid that has a node and at least two communication pencils, and does not require the specific structure of Group I. See MPEP § 806.05(d).

5. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

6. During a telephone conversation with Michael Glenn on 7/30/04, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-30. Affirmation of this election must be made by applicant in replying to this Office action. Claims 31-92 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

#### ***Information Disclosure Statement***

7. The information disclosure statements filed 1/03/2001 and 5/22/2001 fail to comply with 37 CFR 1.98(b)(5), which requires that each publication listed in an IDS must be identified by the date of publication. Cited references that fail to comply with 37 CFR 1.98(b)(5) listed on the above information disclosure statements have been placed in the application file, but the information referred to therein has not considered.

***Specification***

8. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.
9. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.
10. The disclosure is objected to because of the following informalities:
  - a. The appendix submitted by the Applicant is improper. The appendix has not been submitted on a Compact Disc (see MPEP § 608.05, and for Computer program listings (37 CFR 1.96(c)). Therefore, it is requested that the Applicant either submit the appendix on a compact disc, cancel the submission of the appendix, or amend the specification to add the contents of the appendix to the specification.

Appropriate correction is required.

***Claim Objections***

11. Claims 9-10, 14 and claims 23-26 are objected to because of the following informalities:
  - a. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim. A claim that depends from a dependent claim should not be separated by any claim

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that does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n). See claims 8-10, where claim 10 improperly depends on claim 8, while claim 9 depends on claim 5, as well as claims 23-26, where claim 23 improperly depends on claim 6, while claims 8-22 depend on claim 5.

- b. Claim 14 recites the limitation, "containing at least" on its second line. Please correct the language to read, "containing at least" in order to be grammatically correct.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

- 12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- 13. Claims 1-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- 14. Claim 1 recites the limitations, "M orthogonal directions" as well as "M dimensional lattice" on its first and second lines, respectively. It is unclear if M is always the same for both the number of dimensions of the lattice and the number of orthogonal directions. Furthermore, it is unclear which "M" is being referenced in dependent claims 6, 7, 25, 26, 28, and 29 when an "M" is used in an equation within a claim. Please correct the claim language to more clearly

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distinguish between the “orthogonal directions” and “dimensional lattice” so as to define the metes and bounds of the claim. Dependent claims 2-30 contain all of the limitations of their parent claims, and thus are rejected for the same reasons as above.

15. Claim 4 recites the limitation “the number of communications paths required to interconnect each node of said corresponding node pencil directly to the other of said nodes of said corresponding node pencil”. It is unclear how many or which nodes “other of said nodes” is meant to encompass. Please correct the claim language to more clearly define the metes and bounds of the claim. Dependent claims 5-30 contain all of the limitations of their parent claims, and thus are rejected for the same reasons as above.

16. Claim 6 recites the limitation “N” in its second line. There is insufficient antecedent basis for this limitation in the claim. For the purposes of the examination of claim 6 and its dependent claims, the Examiner will assume that N has a value of 3. Dependent claims 7 and 23-26 contain all of the limitations of their parent claims, and thus are rejected for the same reasons as above.

17. Claim 7 recites the limitation “ $M*(N-1)/P$ ” on its third line. It is unclear what portions of the equation are meant to be divided by “P”, whether it is “ $M*(N-1)$ ”, “ $(N-1)$ ” or simply “M”. Please correct the claim language to more clearly define the metes and bounds of the claim.

18. Claim 28 recites the limitation “N” in second line. There is insufficient antecedent basis for this limitation in the claim. For the purposes of the examination and claim 28 and its dependent claims, the Examiner will assume that N has a value of 2. Dependent claim 29 contains all of the limitations of its parent claim, and thus is rejected for the same reasons as above.



***Claim Rejections - 35 USC § 102***

19. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

20. Claims 1-19, and 23-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Bolstad et al., U.S. Patent No. 5,842,034.

21. Regarding claim 1, Bolstad has taught a communications network with M orthogonal directions (50 of Fig.1) supporting communications between an M dimensional lattice (see Fig.1) of a multiplicity of nodes (90 of Fig.1) each containing a multiplicity of ports (see Col.3 lines 5-12), said communications network comprising:

- a. A communication grid interconnecting said nodes, said grid further comprising:
  - I. A multiplicity of communication pencils (C1-C4 and R1-R8 of Fig.1), for each of said M orthogonal directions (see Fig.1 and Col.2 lines 55-62),
  - II. Wherein each of said communication pencils in each orthogonal direction is coupled with a corresponding node pencil containing a multiplicity of nodes (see nodes 90 of Fig.1 connected vertically to each of C1-C4, or nodes connected horizontally to each of R1-R8) to couple each of said nodes of said corresponding node pencil directly to the other nodes of said corresponding node pencil (see Fig.1 and Col.3 line 58 – Col.4 line 9),
  - III. Wherein M is at least two (see Fig.1),

IV. Wherein the number of nodes in each of said node pencils in a first of said orthogonal directions is at least four (see eight nodes 90 of Fig. 1 connected vertically to each of C1-C4),

V. Wherein the number of nodes in each of said node pencils in a second of said orthogonal directions is at least two (see four nodes 90 of Fig. 1 connected horizontally to each of R1-R8).

22. Regarding claim 2, Bolstad has taught the communications network of claim 1, wherein the number of nodes in each of said node pencils in said second orthogonal direction is at least three (see four nodes 90 of Fig. 1 connected horizontally to each of R1-R8).

23. Regarding claim 3, Bolstad has taught the communications network of claim 2, wherein the number of nodes in each of said node pencils in said second orthogonal direction is at least four (see four nodes 90 of Fig. 1 connected horizontally to each of R1-R8).

24. Regarding claim 4, Bolstad has taught the communications network of claim 1, wherein each of said communication pencils is comprised of the number of communications paths required to interconnect each node of said corresponding node pencil directly to the other of said nodes of said corresponding node pencil (see Col.3 line 58 – Col.4 line 9).

25. Regarding claim 5, Bolstad has taught the communications network of claim 1, wherein:

a. Each of said nodes is comprised of P coupled communications processors (see Col.3 lines 6-12 and Col.5 lines 60-67). Here, because each processing element of the node contains a communications interface and communicates with other processing elements, each can be considered a communications processor.

- b. Wherein P is at least two (see Col.3 lines 6-12). Here, even though each node of Bolstad contains 16 processing elements, because each node is "comprised" of P communications processors, P will be considered to be 2.
  - c. Wherein each of said communications processors is coupled to at least one of said communication pencils (see Col.3 lines 6-12, Col.4 lines 18-24 and Col.5 lines 37-43, 60-67). Here, because the processing elements of each node are connected via the communication interfaces of each PE (see Col.5 lines 37-43, 60-67), and the nodes are connected to a communication pencil in each orthogonal direction (see Fig.1), each processing element is therefore coupled to both of the communication pencils.
26. Regarding claim 6, Bolstad has taught the communications network of claim 5, wherein P is a factor of  $M*(N-1)$ . Here, M has a value of two (see Fig.1 and Col.2 lines 55-62), N has a value of three (see above paragraph 16), and P has a value of two (see above paragraph 25). Two is a factor of two, and thus P is a factor of  $M*(N-1)$ .
27. Regarding claim 7, Bolstad has taught the communications network of claim 6, wherein each of said coupled communications processors comprises at least  $M*(N-1)/P$  ports. Here, M has a value of two (see Fig.1 and Col.2 lines 55-62), N has a value of three (see above paragraph 16), and P has a value of two (see above paragraph 25). Each communications processor has two ports (see Col.5 lines 37-44), and thus each communications processor has  $M*(N-1)/P$  ports.
28. Regarding claim 8, Bolstad has taught the communications network of claim 5, wherein at least one of said communications processors (120 of Fig.5) is further comprised of at least one instruction processor (120A of Fig.5) accessibly coupled to a memory (120B of Fig.5) (see Col.5

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lines 60-67). Here, it is inherent that the CPU (120A of Fig.5) coupled to a memory (120B of Fig.5) of each processing element (120 of Fig.5) is able to execute instructions to perform operations on data.

29. Regarding claim 9, Bolstad has taught the communications network of claim 5, wherein each of said communications processors (120 of Fig.5) is further comprised of at least one instruction processor (120A of Fig.5) accessibly coupled to a memory (120B of Fig.5) (see Col.5 lines 60-67). Here, it is inherent that the CPU (120A of Fig.5) coupled to a memory (120B of Fig.5) of each processing element (120 of Fig.5) is able to execute instructions to perform operations on data.

30. Regarding claim 10, Bolstad has taught the communications network of Claim 8, wherein:

- a. Wherein each of said communications processors is comprised of a communications instruction processor accessibly coupled to said memory (see Col.5 lines 60-67). Here, because each processing element can be considered both a communications processor (see Col.3 lines 6-12 and Col.5 lines 60-67, as well as above paragraph 25) and an instruction processor (see above paragraph 28), each processing element is inherently comprised of a communications instruction processor.
- b. Wherein said communications instruction processor is communicatively coupled to at least one of said ports (see Col.5 lines 37-43).

31. Regarding claim 11, Bolstad has taught the communications network of claim 10, wherein said instruction processor acts as said communications instruction processor (see Col.3

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lines 6-12 and Col.5 lines 60-67, as well as above paragraphs 25 and 28). Here, because the instruction processor (120A of Fig.5) is comprised within a communications instruction processor (120 of Fig.5), and because the CPU (120A of Fig.5) communicates with other processing elements via the communication interface (see Col.5 lines 37-43, 60-67), the CPU (120A of Fig.5) inherently acts as a communications instruction processor.

32. Regarding claim 12, Bolstad has taught the communications network of claim 10, wherein each of said communications instruction processor (120 of Fig.5) and said instruction processor (120A of Fig.5) reside in a single package (see Fig.5).

33. Regarding claim 13, Bolstad has taught the communications network of claim 10, wherein said accessibly coupled memory (120B of Fig.5) comprises a memory module (see Col.5 lines 60-67).

34. Regarding claim 14, Bolstad has taught the communications network of claim 10, wherein each of said nodes further comprises a package containing at least two of said communication processors (see Col.3 lines 5-12).

35. Regarding claim 15, Bolstad has taught the communications network of claim 14, wherein at least one of said communications processors in said package comprises an instruction processor (120A of Fig.5) accessibly coupled to at least one memory (120B of Fig.5) (see Col.5 lines 60-67). Here, it is inherent that the CPU (120A of Fig.5) coupled to a memory (120B of Fig.5) of each processing element (120 of Fig.5) is able to execute instructions to perform operations on data, and because each processing element of the node contains a communications interface and communicates with other processing elements, each can also be considered a communications processor.

36. Regarding claim 16, Bolstad has taught the communications network of claim 15, wherein said package comprises said accessibly coupled memory (see Fig.5 and Col.3 lines 5-12). Here, because each processing element contains an accessibly coupled memory, a package that contains multiple processing elements inherently contains an accessibly coupled memory.

37. Regarding claim 17, Bolstad has taught the communications network of claim 15, wherein said accessibly coupled memory is comprised of an external memory circuit (120B of Fig.5) accessibly coupled to at least one of said instruction processors (120A of Fig.5). Here, the memory system of each processing node contains a memory system separate from the CPU core (see Fig.5 and Col.5 lines 59-67).

38. Regarding claim 18, Bolstad has taught the communications network of claim 8, wherein said communications processors are coupled by a bus (see Col.5 lines 27-43).

39. Regarding claim 19, Bolstad has taught the communications network of claim 18, wherein at least one of said nodes is further comprised of a bus arbitration scheme controlling said bus coupling (see Col.5 lines 27-43). Here, it is inherent that there is some sort of bus arbitration scheme controlling the bus connections in between the processing elements, as without some sort of scheme, the connections would be useless.

40. Regarding claim 23, Bolstad has taught the communications network of claim 6, wherein  $N-1$  is a factor of  $P$ . Here,  $M$  has a value of two (see Fig.1 and Col.2 lines 55-62),  $N$  has a value of three (see above paragraph 16), and  $P$  has a value of two (see above paragraph 25). Two is a factor of two, and thus  $(N-1)$  is a factor of  $P$ .

41. Regarding claim 24, Bolstad has taught the communications network of claim 23, wherein  $P$  is equal to  $N-1$ . Here,  $M$  has a value of two (see Fig.1 and Col.2 lines 55-62),  $N$  has a

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value of three (see above paragraph 16), and P has a value of two (see above paragraph 25).

Two is equal to two, and thus P is equal to N-1.

42. Regarding claim 25, Bolstad has taught the communications network of claim 6, wherein M is a factor of P. Here, M has a value of two (see Fig. 1 and Col. 2 lines 55-62), N has a value of three (see above paragraph 16), and P has a value of two (see above paragraph 25). Two is a factor of two, and thus M is a factor of P.

43. Regarding claim 26, Bolstad has taught the communications network of claim 6, wherein P is equal to M. Here, M has a value of two (see Fig. 1 and Col. 2 lines 55-62), N has a value of three (see above paragraph 16), and P has a value of two (see above paragraph 25). Two is equal to two, and thus M is a factor of P.

44. Regarding claim 27, Bolstad has taught the communications network of claim 5, wherein said communications processors are coupled by a direct connection network to each of said communications processors coupled directly to each of the remaining of said communications processors (see Col. 5 lines 37-43, 60-67).

45. Regarding claim 28, Bolstad has taught the communications network of claim 4, wherein each of said nodes comprises  $M*(N-1)$  ports (see Col. 3 lines 5-12). Here, M has a value of two (see Fig. 1 and Col. 2 lines 55-62) and N has a value of two (see above paragraph 18). Each node has two external ports (see Col. 3 lines 5-12), and thus each node comprises  $M*(N-1)$  ports.

46. Regarding claim 29, Bolstad has taught the communications network of claim 28, wherein at least one of said nodes comprises more than  $M*(N-1)$  ports. Here, M has a value of two (see Fig. 1 and Col. 2 lines 55-62) and N has a value of two (see above paragraph 18). Each node has two external ports (see Col. 3 lines 5-12) as well as 2 internal ports connecting the

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processing elements (see Col.5 lines 37-44), and thus at least one of the nodes comprises more than  $M*(N-1)$  ports.

47. Regarding claim 30, Bolstad has taught the communications network of claim 4, wherein:

- a. At least one of said nodes is comprised of a coupled communications processor (see Col.3 lines 6-12 and Col.5 lines 37-43, 60-67). Here, because each processing element of the node contains a communications interface and communicates with other processing elements, each can be considered a communications processor.
- b. Said communications processor is coupled to each of said communication pencils (see Col.3 lines 6-12, Col.4 lines 18-24 and Col.5 lines 37-43, 60-67). Here, because the processing elements of each node are connected via the communication interfaces of each PE (see Col.5 lines 37-43, 60-67), and the nodes are connected to a communication pencil in each orthogonal direction (see Fig.1), each processing element is therefore coupled to both of the communication pencils.

***Claim Rejections - 35 USC § 103***

48. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.



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49. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bolstad et al., U.S. Patent No. 5,842,034 as applied to claims 1, 4-5, 8 and 18-19 above, and further in view of Patterson et al., *Computer Organization & Design: The Hardware/Software Interface* (hereinafter Patterson).

50. Regarding claim 20, Bolstad has taught the communications network of claim 19, but has not explicitly taught wherein said bus arbitration scheme controlling said bus coupling supports a bus master.

51. However, Patterson has taught the use of a processor as a bus master to arbitrate and control requests to the bus so that multiple processors on a bus can request and obtain data in a fair and correct manner (see Patterson, p.667-670). Because it is desirable to have correct results and to avoid processors being unfairly excluded from bus access, one of ordinary skill in the art would have found it obvious to modify the communications network of Bolstad to use a processor as a bus master to control requests to the bus so as to provide correct results in a fair manner.

52. Regarding claim 21, Bolstad in view of Patterson has taught the communications network of claim 20, wherein said bus master is one of said communications processors (see Patterson, p.667-670 and above paragraphs 50-51).

53. Regarding claim 22, Bolstad in view of Patterson has taught the communications network of claim 21, wherein said bus master can over time be any of said communications processors (p.667-670 and above paragraphs 50-52). Here, any device that submits bus requests can be a bus master, and inherently over time anyone of the processing elements within a node of Bolstad

will submit bus requests to communicate with the other processing elements within the node. Thus, over time, any of the processing elements could be the bus master.

### ***Conclusion***

54. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

55. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

56. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER  
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